REMARKS

Claims 1-10 are pending in the present application and stand rejected. Claims 1, 3-5 and 8-10 have been amended to correct minor editorial errors. The Examiner's reconsideration of the claim rejections is respectfully requested in view of the following remarks.

Drawing Objections

The drawings stand objected. Corrected drawings in accordance with the Examiner's suggestions are attached herewith. Particularly, the legend "(Prior Art)" has been designated in Figures 1-5. Additionally, arrows have been added to boxes 1130, 1140, 1170, 1180, 1190 and 1195. Arrow heads have been added to connections in boxes 1110, 1150 and 1160. Withdrawal of the objections to the drawings is respectfully requested.

Specification Objections

The specification stands objected. The specification has been amended above in accordance with the Examiner's suggestions. Withdrawal of the objections to the disclosure is respectfully requested.

Claim Objections

Claims 1-10 stand objected. The claims have been amended above in accordance with the Examiner's suggestions. Withdrawal of the objections to the claims is respectfully requested.

Claim Rejections under § 112

Claims 1-10 stand rejected under 35 U.S.C. § 112, second paragraph, for:

(a) "result field" in claims 1, 2, 8, 9 and 10;

(b) "so-called 'extract' instruction" in claim 1; and

(c) "a first smaller bit-length instruction" in claims 1, 8, 9 and 10.

Regarding (a), claims 1, 8, 9 and 10 have been amended to clarify "the instruction" as "the extract instruction. The "extract instruction" is disclosed as a "so-called" extract instruction that "writes the 'overhanging' *bit portion* not into its own result field but in the result field of the subsequent...instruction." (Specification, paragraph [0049]). The claimed "extract instruction" does not conflict with the disclosure provided in the Patterson and Hennessy reference. Regarding (b), claim 1 has been amended in accordance with the Examiner's suggestion. Regarding (c), claims 1, 8, 9 and 10 have been amended to claim "a first instruction." Withdrawal of the rejection of claims 1-10 under 35 U.S.C. § 112, second paragraph, is respectfully requested.

Claim Rejections under § 103

Claims 1-5 and 7-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mahurin et al. (U.S. Patent No. 6,493,819) (hereinafter "Mahurin") in view of Isaman (U.S. Patent No. 6,449,710) (hereinafter "Isaman"), and Superscalar Microprocessor Design by Johnson (hereinafter "Johnson") and Computer Organization and Design by Hennessy and Patterson (hereinafter "Hennessy"). The rejections are respectfully traversed.

Claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mahurin, Isaman, Johnson and Hennessy, and further in view of White et al. (U.S. Patent No. 5,574,928) (hereinafter "White") and Gover et al. (U.S. Patent No. 5,752,062) (hereinafter "Gover"). The rejections are respectfully traversed.

Claim 1 claims, *inter alia*, "adding an extract instruction into an instruction stream *before the first instruction.*" The Office Action relies on col. 5, lines 47-48 of Mahurin, which states "a read of the destination will be done prior to the execution of the instruction." The recited portion of Mahurin is patentably distinguishable from the recited portion of claim 1. In particular, "a read of the destination" requires adding a source operand to the instruction (i.e., reading one more operand), whereas "adding an extract instruction into an instruction stream" does not require adding a source operand. Adding the source operand requires extra hardware, which may be prohibitively expensive in the presently claimed invention.

Claim 1 further claims, *inter alia*, "writing the extract instruction result into the *result field of said first instruction.*" As noted above, the first instruction is after the extract instruction in the instruction stream. The recited portions of Mahurin and Isaman do not teach or suggest the recited limitations of claim 1. In particular, the recited portions of Mahurin teach writing to a destination register and not a "*result field of said first instruction.*"

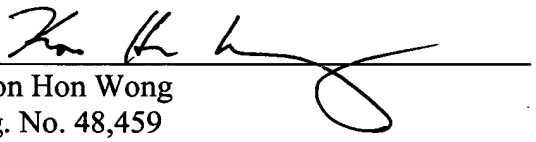
It should be noted that a result of claim 1 is that an extract instruction is introduced that writes its result in the same reorder buffer (ROB) as the "smaller bitlength" instruction immediately following it. The combination of Mahurin and Isaman does not teach or suggest two instructions writing to the same ROB.

It should also be noted that the teachings of Isaman are dismissed in paragraph [0045] and Figure 6 because of potential performance loss. That is, Isaman introduces dependencies between the smaller bit-length instructions, the stitch instruction, and the instructions consuming the target register (e.g., Figure 1 -- ADD, STITCH LOW, STITCH HIGH, and SUB).

Independent claims 8, 9 and 10 are believed to be allowable for at least the reasons provided for claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. Withdrawal of the rejection of claims 1-10 under 35 U.S.C. §103(a) is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

By: 

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